A 100 MHz TIME-TO-DIGITAL-CONVERTER SYSTEM IN VMEbus

Peter von Walter, Jürgen Engelfried
Physikalisches Institut
University of Heidelberg
Philosophenweg 12
D-6900 Heidelberg
Tel.: 06221/569380
EARN/BitNet: vWalter@DHDPHY5

ABSTRACT

A new designed multi-channel (18 channels), multi-hit (<255) and multi-event (<255) Time-to-Digital-Converter (TDC) system, consisting of Discriminator- and TDC-modules, is described. The TDC with a time resolution of 10ns is designed for a RICH detector and optimized for fast readout at high event rates. To achieve high speed throughput the system is built up in VMEbus for full 32 bit data transfer in combination with powerful VME processor modules for data processing. All timing, channel and module information in several modules in the VME crate can be read out by one block transfer.

INTRODUCTION

A new readout system for a new hyperon beam experiment (WA89) using the OMEGA facility at CERN [1] has been designed and built at the Physics Institute of Heidelberg. The system has to handle 1280 channels from the UV-detecting chambers of a RICH (Ring Imaging CHerenkov) counter, which have to be read out very fast (<50µs) for trigger purposes, and 576 channels from the drift chambers in the decay region, which can be read out slower (no triggering). The whole system (excluded the preamplifiers) will host in VME. It will consist of 3 parts: discriminators, Time-to-Digital-Converters (TDCs) and microprocessors [2].

This paper describes the detector physics, the experimental setup with its readout scheme and the Discriminator modules and the TDC modules in detail, which are optimized for multihit detection and fast readout of data.

PHYSICS

The new hyperon beam experiment (WA89) will investigate the following topics:

- production and decay of charmed-strange baryons
- verification and investigation (if it exists) of the U(3100), an exotic state possibly consisting of two quarks and two antiquarks
- search for the double-strange dibaryon H
- study Ξ and Ω resonances

The particles are produced with an 360 GeV/c Hyperon beam, consisting of π^- and Σ^- with ratio 2/1, with some percent Ξ^-, and some Ω^-, produced with 450 GeV protons from the CERN SPS. All these states will decay into (at least one) Lambda, Kaon and Protons, and Pions. For example, the Ξ_c^+ (quark content csu) has been observed in the channel

$$\Xi_c^+ \rightarrow \Lambda^\circ K^- \pi^+ \pi^+ \quad [3], \qquad (1)$$

and the U in the channels

$$U \rightarrow \Lambda^\circ + \bar{p} + \pi's \quad [4,5]. \qquad (2)$$

To identify these states, one have to reconstruct the Λ° (decaying into p π^-) and one has to discriminate a high momentum negative particle (K- or $\bar{p}$) against π's for momenta up to 150 GeV/c. The leading negative particle will be most probable not a π^-, so this criteria should be build into the trigger. A principle layout of the experiment is shown in fig.1.

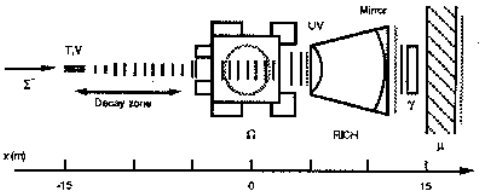

Fig.1: Detector Layout of the WA89 experiment

The momenta of the (charged) particles are determined by the curvature of the tracks inside the Omega Magnet with a bending power of 8 Teslameter. A decay zone equipped with driftchambers to detect the Λ°s is situated upstream the magnet. Downstream a RICH detector is used to determine the velocity of the charged particles. In addition, a electromagnetic calorimeter is needed to identify π°.

The data are taken in a spill structure. The SPS delivers the protons for ≈2sec, with a 15sec cycle time. In the 2sec (on spill) we expect ≈10k first level triggers 500nsec after the interaction, which will be reduced by slower decisions within 300µsec to <1000 with the aid of a special trigger system (MBNIM), which also delivers track information for the

Block Data Transfer

The read out of the TDCs will be done in block transfer mode with aid of the daisy chained IACKIN/IACKOUT lines on the VME backplane. Each module therefore knows when to take over in the block transfer from its left neighbour. Only modules with valid data will participate in the block transfer. For the processor these data look like one contiguous block where the end of the block transfer will be signaled (by interrupt or BusError) by the most right TDC module in the crate.

Each 32 bit word holds the information of one "hitslice": 10 bits time, 18 bits channel pattern and 4 bits for the module number. Fig.11 shows a typical memory layout of one TDC module.

Addr	Channel0 ... Channel17 D31 ... D14	Time D13 ... D4	Mod# D3 D0	
0	01010000010000000	0000100000	0100	
1	00000000000000000	1111111111	0100	TCO
2	00000001100000100	0000000100	0100	
3	00000000000100000	0000001100	0100	
4	11000000100000100	1111111111	0100	TCO
252	00000000000000010	0000001000	0100	Stop
253	00010000000100100	0000100000	0100	HC
254	00000000000000000	1111111111	0100	
255	00000000100100111	0000001000	0100	

TCO = TimeCounter Overflow; Stop = StopMarker; HC= HitCounter;

Fig.11: Typical memory content of TDC-module

In COMMON START mode only addresses below the current hit counter (after stop) contain valid data. The hitcounter on every module therefore determines the amount of data each module contributes to the block transfer.

In COMMON STOP mode the position of the hitcounter in each module is random. To avoid the readout of all data per module (256 words!) the time information itself has to be scanned to stop for the valid time range. In the present design a special data monitor module in the crate watches the data in the block transfer to switch control to the next TDC module for participating in the block transfer.

Each crate is connected to its own microprocessor for parallel readout, with these microprocessors hosted together in a special VME crate. We are aiming for a readout time of less than 500 ns per "hitslice". For 16 TDC modules in one VME crate with approximately 5 hits/module this results in a total readout time of 40 µs for the whole system.

PRESENT STATE

Presently a subsystem of 90 discriminator modules and 90 TDC modules for 1440 analog channels has been build up and successfully tested.

REFERENCES

[1] A. Forino et al., "Proposal for a new hyperon beam experiment at the CERN-SPS using the Omega facility", CERN/SPSC-87/43, SPSC-P/233, 27.Aug.1987

[2] J. Engelfried, "The readout of the Omega RICH and the decay region chambers for WA89", Internal Memorandum, Oct. 17,1988

[3] S.F. Biagi et al., Phys. Lett. 122B(1983) 455

[4] M. Bourquin et al., Phys. Lett. 172B(1986) 113

[5] A.N. Alcev et al., JINR Rapid Communications No. 19-86

[6] Kommt noch

[7] P .v. Walter, "A Data-Acquisition-System in VMEbus with 100 MHz Flash-ADCs", IEEE Trans. Nucl. Science, Vol. 35, No. 1, Feb. 1988

The principle of this circuitry with a two bit shift register and a coincidence gate can be seen in fig.8.

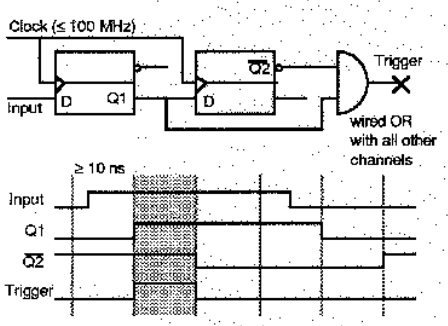

Fig.8: Trigger Circuitry for leading edge detection

These signals are now synchronized to the clock and also represent a channel data pattern for the input pulses which started in the current time slice of 10ns. All signals are also combined ('OR-ed') to form a general trigger which causes the writing of the current time to the TIME MEMORY and of the current channel pattern to the CHANNEL MEMORY.

After recording the hit (on one or more channels), the HIT COUNTER, which determines the address to the RAMs, will be incremented by one and the circuit waits for the next hit. On overflow of the time counter (after 10µs) a marker hit with this time (=1023) will be stored. If there is also a real signal trigger at this moment the according channel pattern is recorded the same way. Therefore no hits will be lost and the full time range (until the hit counter overflows) can be reconstructed (see also Fig.11 for memory layout)!

The CONTROL LOGIC in the TDC module handles all the control signals (START, STOP, RESET) and delivers status (BUSY, HIT) and timing signals for the circuitry. All control and status signals can either be supplied externally or initiated and tested by software. In principle there are two main recording modes available (as shown in fig.9 and fig.10) which can be programmed in several aspects through some mode bits in a command register on the TDC:

Bit8	AutoStop on Time Counter Overflow: for a recording length of 10µs (100 MHz clock)
Bit9	AutoStop on Hit Counter Overflow: to assure that no hits will be overwritten!
Bit10	Gated Mode: The START signal serves as a combined START/STOP signal (GATE) for simplicity. No Stop Marker will be written! The STOP signal is disabled.
Bit12	Trigger Mode: The STOP signal serves as an external TRIGGER signal (leading edge) to initiate the writing of a hit with time and channel information. Stop either on AutoStop or in Gated Mode!

Table 1: Mode bits in DL501 command register

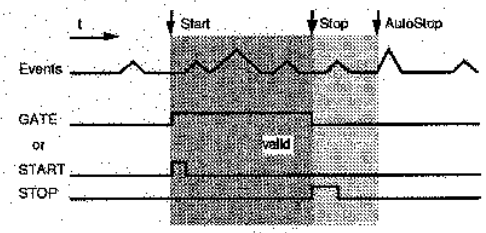

Fig.9: COMMON START recording mode

Fig.9 shows the typical COMMON START mode where after an early experiment trigger the recording of following events continues until either the module is stopped by an external signal (STOP, end of GATE) or an AutoStop on time counter overflow or hit counter overflow. The HIT COUNTER can be read out to see how many hits are accumulated!

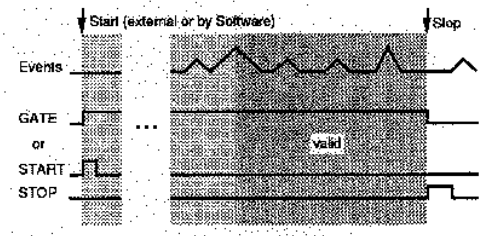

Fig.10: COMMON STOP recording mode

In many cases it is not possible to provide an early start signal for the TDC. The events occure before a general experiment trigger is available and have to be recorded in advance. Fig.10 shows the COMMON STOP mode where the TDC is already running and will then be stopped by an external signal after the events. The memory is therefore filled with the prehistory which can be reconstructed unambigously. (through the recording of time overflow markers!) up to 2.7ms.

Data Readout

The RAMs have a depth of 256 words, so hitpatterns of 256 different timings can be accumulated. There is no conversion time and only valid data are recorded to fulfill the requirements for fast readout. The data has to be read out sequentially in reverse order where the hitcounter will be decremented automatically to point to the current hitslice. The hitcounter can always be read out to give the number of remaining data.

Based on a VME module already designed, built and tested in our institute [7] a new design has been undertaken to optimize the readout also with block transfer.

channel VME board and how the channel submodules are interconnected.

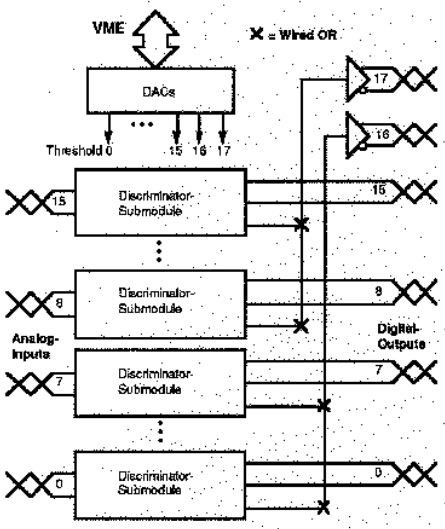

Fig.5: Blockdiagram of DL504 Discriminator board

The threshold of every input channel 0...15 can be programmed independently and determines the appropriate output. The signals from the second threshold (common threshold 16 and 17) are combined in two groups of 8, with one common output per group. This gives 18 differential ECL signal outputs from the discriminator module, which are transmitted via twisted pair cables to the TDC modules 40 meters away.

TDC MODULES

Fig.6 shows the TDC module (DL501) in VME which houses 18 channels accordingly. The provisions for the -5.2 Volt supply are the same as for the DL504 Discriminator module.

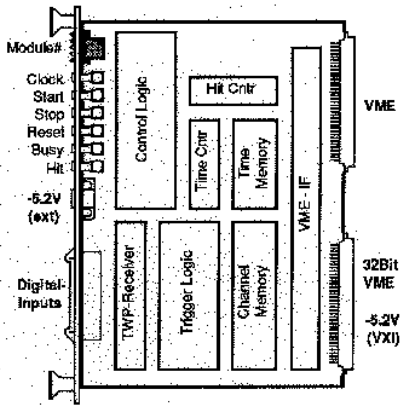

Fig.6: Layout of DL501 Time-to-Digital-Converter board

The digital inputs are differential ECL signals, all other control and status signals are in NIM standard. To understand the functions of the TDC module refer to the blockdiagram in Fig.7.

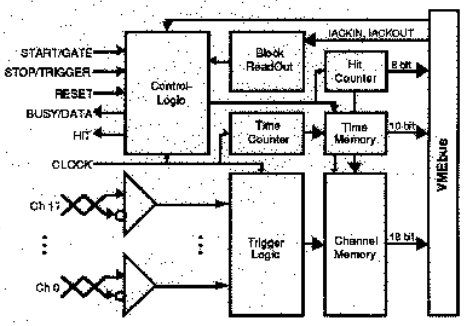

Fig.7: Blockdiagram of the DL501 TDC

The system CLOCK of ≤100 MHz can be either generated by an onboard quartz oscillator or has to be supplied (for a multi module system) from the front. This clock is counted by a TIME COUNTER (10 bits) and determines the basic time resolution of 10 ns.

A special digital differen ation circuitry (TRIGGER LOGIC) for every input channel detects the starting of an input pulse and outputs a channel signal for the rising edge of each signal.

output of the discriminators is then transported via twisted pair cables to the TDCs, which are situated in the counting baraque together with the electronics for the other detectors of the Omega facility.

For the 1280 sense wires of the RICH detector and 16 channels per module, we need 80 discriminator and 80 TDC modules. These modules will be distributed over 6 crates to have the same amount of data in each crate, with a maximum of 16 modules in one crate. Each crate is connected via a VME-VSB interface (DL502) to its own microprocessor (with VSB port). For parallel readout these hit processor boards (HiP1-6) are housed together in a special VME crate. The TDC modules for the decay region chambers (576 channels) are sitting in 3 Crates together (DL502) and are connected to another hit processor (HiP7). For this detector, no fast readout for trigger purposes is needed, therefore only the interfaces are planned digitally.

In the microprocessor crate, one additional track processor (TraP) is controlling the whole crate, calculating the track coordinates for obtaining the ring centers and writing the data off spill via a Fastbus-VSB-Interface (FVSBI) to a Fastbus crate. Here the data are combined with the other detectors and written via a microVAXIII to tape. In total there are 8 microprocessors involved. We are using the processor boards from CES (FIC8230) with a 24Mhz 68020 microprocessor,1 MByte static DRAM and DMA Controller.

If there is a trigger, the system will do the following: The TDCs for the RICH are started (Common Start), and the already running TDCs for the decay region are stopped (Common Stop). After 8µsec (maximum drift time in the RICH drift chamber) the readout of the TDCs is started in block transfer mode on 7 HiPs in parallel. The readout will be finished after ≤50µsec for the RICH and ≈300µsec for the decay region. In the meanwhile the TraP receives the first coordinates of the leading particle and distributes it to the HiPs. They will calculate the radius and the TraP can decide, whether this particle is a pion. The TraP will then generate a FastClear signal to the rest of the experiment. During all this activities, the system can receive a FastClear from the main trigger system. All data from one spill are stored in the HiPs. Off spill, the TraP collects the data from the HiPs and writes it over the VSB port to a FVSBI, sitting in a fastbus crate[6].

In the following the different frontend modules are described in detail.

DISCRIMINATOR MODULES

For reasons of modularity , flexibility and also to minimize problems of transmission of analog signals over long distances, the discriminators for the analog signals from the preamplifiers (which sit directly at the detectors) are housed in a special VME module. Fig.3 shows this board (DL504) with 16 channels.

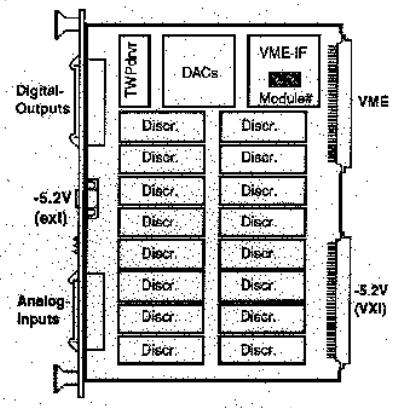

Fig.3: Layout of DL504 Discriminator board

For fast ECL based electronics a highpower -5.2V supply is essential. Unfortunately this is not provided in the VME standard and therefore has to be forseen additionaly. One supported solution is to use the outer row pins of the connector P2 (User I/O) as proposed by the new VXI standard. This needs an appropriate P2 backplane in the crate. For standard VME crates the -5.2 Volt can also be fed in from the front.

The discriminators are configured as replacable submodules to adapt for different applications (e.g. the Twisted Pair receiver does an additional amplification by factor 3). The schematic for the submodule is shown in fig.4.

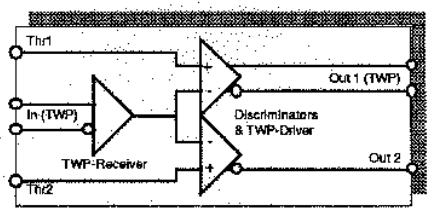

Fig.4: Discriminator Submodule for one channel

Each channel has two comparators with separate thresholds in order to distinguish between the pulse originating from a photoelectron and the dE/dx signal of a passing charged particle. Fig.5 shows the blockdiagram of a complete 16

leading particles. During spill, the data is collected in fast memories, which are read out off spill. This is necessary, because the rate is limited by the writing to tape.

RICH detector

If a particle is passing through a medium with a velocity greater than the speed of light in this medium, light is emitted under a certain angle respective to the particle track (Cherenkov effect). The angle theta is given by

$$\cos(\Theta) = \frac{1}{v/c \cdot n} \qquad (3)$$

with v the particle velocity, c the speed of light in vacuum and n the refractive index of the medium.This light (mostly UV photons) is focused by spherical mirrors to a circle with radius r, which is given (for small angles) by

$$r = \Theta \cdot \frac{L}{2} \qquad (4)$$

where L is the radius of curvature of the mirrors. For our setup with a focal length of 5m, the maximum radius for very fast particles ($\beta \rightarrow 1$) will be 85mm. At 160 GeV/c, this leads to a radius difference between Kaons and pions of

$$(\Delta r)_{\pi,K} = 1.3\text{mm}. \qquad (5)$$

The centers of the rings will be distributed over an area of approx. 120cm horizontal and 40cm vertical.

To measure the impact of the photons, a UV sensitive driftchamber of 160cm·80cm and 6cm thickness is installed in the focal plane. The counting gas is ethan with some ppm of Tetra-kis-Methyl-Ethylen (TMAE) to produce electrons via photoeffect at atmospheric pressure, operated at saturated drift velocity. The absorption length for photons is ≈1cm. With the high voltage electrode in the middle of the chamber, the photelectrons are drifting upwards or downwards respectively to the sense wires, with a maximum drift path of 40cm and a velocity of approx. 5cm/µsec. The impact point of the photon is than determined by the wire and by the drift time to this wire, where the electron arrives. In addition to the photoelectrons, much more electrons (some hundred) are produced via the dE/dx signal of the passing particle itself. With 14 photoelectrons per ring, the position of one electron has to be measured with an accuracy of $\sigma \leq 1.5$mm, in order to be able to separate K and π at 160GeV/c with 4 std.dev. The main contribution to the space resolution is due to diffusion, which has a $\sigma \approx 1$mm transversal and longitudinal to the drift direction. The wire spacing is 2.54mm, leading to a total number of 1280 readout channels.

The electronic for this detector must fulfill the following conditions:

- measure the drift time with an accuracy of $\sigma \leq 5$nsec
- discriminate between a single photoelectron and the electrons from the dE/dx signal
- more than one electron can arrive at the same wire (overlapping rings)
- more than one electron can arrive at the same time at different wires
- fast readout (≈50µsec) to use the information about the leading particle already on the trigger level
- time measurement can be started with the first level trigger signal

Lambda chambers (Decay region)

These chambers are normal drift chambers with a maximum drift time of 500nsec and a space resolution of ≈300µm, operated with a mixture of Ethan, Methane and Isobutan 88/10/2. The drift time has to be measured to an accuracy of $\sigma \leq 5$nsec. These detectors have together 576 sense wires. Due to the short drift time, the time measurement has to be stopped with the trigger signal in order not to loose any information.

READOUT SYSTEM

The general layout for the readout system is shown in fig.2.

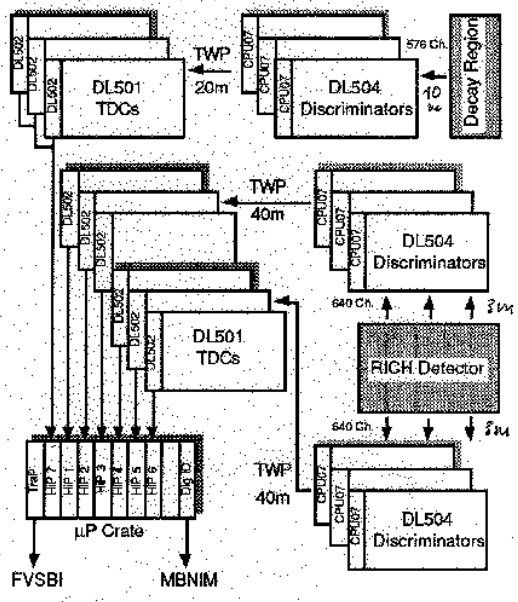

Fig.2: Readout system for WA89 experiment

Most of the electronics is housed in a baraque 40m (RICH) and 20m (decay region) away from the detectors. To avoid the transmission of analog signals over these long distances, the discriminators are placed near the detectors. For the RICH the distance is only 3m, for the decay region it is 10m. The digital